FABRICATION OF AN ATOM CHIP

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Masters Report

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Introduction

The investigation of quantum gases has developed rapidly since the realization of a Bose-Einstein Condensate (BEC) in 1995 [1], and that of a Fermi-Degenerate Gas (FDG) in 1999 [2]. Because of the high level of control achievable, quantum gases are a useful model of condensed matter systems such as the Superfluid to Mott-insulator phase transition [3,4], BEC-BCS crossover physics [5], and quantum simulation [6], among others. The Thywissen group has built an experiment [7] that hopes to probe much of the physics related to these phenomena.

A distinguishing feature of our experiment is the use of an atom chip to magnetically trap atoms after they have been laser-cooled. This makes a strongly confining potential possible, allowing for the study of low-dimensional gases [8,9]. The chip currently in use was fabricated by J. Esteve of the Aspect Group in Orsay. For many reasons, it is desirable to be able to design and fabricate a chip within the Thywissen group, and this report details my progress towards this effort.

The project has been a continuation of the work started by Micha Strauss in 2003 [10] and Barabara Cieslak in 2004 [11] at the Emerging Communications Technology Institute (ECTI) at the University of Toronto. Though much effort had been spent on their parts trying to come up with a successful fabrication procedure, a solution remained elusive. Beginning in December, I took over this work and was able to develop a reliable fabrication technique that produced a new atom chip for our experiment. Furthermore, a numerical model was created of the chip’s magnetic trapping potential and high frequency connections between lead wires and chip contacts were made and characterized.
The first section of the report presents some background theory related to quantum gases and the magnetic trapping of neutral atoms. The second section explains the function of, and motivation for, the various design features of the new chip. In the third section, the fabrication process is described. The fourth section looks at how this new chip is to be coupled into the present system. Finally, the last section contains a summary of all that has been accomplished and the future work to be done.

1. Background Theory

1.1 Quantum Gases and Magnetic Trapping

In order to create a quantum gas, the phase-space density must satisfy the inequality

\[ n_0 \lambda_{db}^3 \geq 1, \]

1.

Where \( n_0 \) is the peak particle density and \( \lambda_{db} = \left( \frac{2\pi\hbar^2}{mk_B T} \right)^{1/2} \) is the de-Broglie wavelength of the particles. This inequality is achieved with low temperature and high density, once the particle has been chosen.

In order to lower the temperature sufficiently, atoms are first cooled with a Magneto-Optical trap (MOT). This involves two counter-propagating, red-detuned, circularly polarized laser beams in each dimension, in the presence of a uniform magnetic field in each dimension. Details of this procedure are described in Marcius Extavour’s Masters Report [12]. The atoms are then transferred to the atom chip where they are magnetically trapped and evaporatively cooled. The details of this procedure may be found in Lindsay LeBlanc’s Masters Report [13].

The magnetic trapping potential of an atom with magnetic dipole moment \( \vec{\mu} \) in a magnetic field \( \vec{B} \) is given by:

\[ U = -\vec{\mu} \cdot \vec{B}. \]

2.
Quantum mechanically, this potential may be written as

$$U = g \mu_B m_F B,$$

where $\mu_B$ is the Bohr magneton, $m_F$ is the component of the total angular momentum $F = J + I$ along the direction of the magnetic field, $B$ is the magnitude of the field, and $g$ is the Lande g-factor given by:

$$g = 1 + \left( \frac{J(J+1) + S(S+1) - L(L+1)}{2J(J+1)} \right) \left( \frac{F(F+1) + J(J+1) - I(I+1)}{2F(F+1)} \right).$$

The sign of the quantity $g m_F$ determines whether an atom is a strong-field seeker ($g m_F < 1$) or a weak-field seeker ($g m_F > 1$). In particular, $^{87}$Rb in the $F = 2, m_F = 2$ sub-level of the $5S_{1/2}$ ground state has $g m_F = 1$, and $^{40}$K in the $F = 9/2, m_F = 9/2$ sub-level of the $4S_{1/2}$ has $g m_F = 1$. Therefore, both $^{87}$Rb and $^{40}$K may be trapped in a magnetic potential minimum.

### 1.2 Magnetic Field from an Atom Chip

An atom chip has a series of wire patterns on its surface. A magnetic trap is produced when current is passed through these wires, creating a field according to the law of Biot-Savart:

$$\vec{B} = \frac{\mu_0 I}{4\pi} \int \frac{d\vec{l} \times \hat{r}}{r^2},$$

where $I$ is the magnitude of the current, $d\vec{l}$ points along the direction of the current, and $\hat{r}$ is the unit vector from $d\vec{l}$ to the field point. A particularly useful result of this law gives the magnetic field from a finite-length, infinitely-thin wire segment:
In the limit $\theta_2 \to \pi / 2$, $\theta_1 \to -\pi / 2$, the result for the infinitely-long, infinitely-thin wire is recovered:

$$B = \frac{\mu_0 I}{2\pi d}. \quad 7.$$

If another magnetic field is then directed perpendicular to this wire segment, a magnetic field minimum is produced where the two fields cancel, creating a trap for weak-field seeking atoms. Confinement along the third dimension requires either a current-carrying wire segment on the chip plane, perpendicular to the original wire segment, and/or a field parallel to the original wire segment that is produced by external coils.

### 1.3 General Properties of Magnetic Traps

There are several properties of magnetic traps that are important to be aware of when designing a magnetic potential:

i) Trap Depth

In order to trap laser-cooled atoms without significant atom loss (due to energetic atoms “jumping” over the trap barrier), the depth of the magnetic trap must be larger than the thermal energy of the atoms by some factor $\eta$:

$$U_{\text{max}} = |\mu B| > \eta k_B T, \quad 8.$$

with $\eta = 3 - 5$. 

$$B = \frac{\mu_0 I}{4\pi d} \left(\sin \theta_2 - \sin \theta_1\right), \quad 6.$$
ii) Effective Trap Volume

The effective trap volume provides an approximate measure of the trap space available. The effective volume can be determined by starting from the Boltzmann density distribution in a magnetic potential:

\[ n(x, y, z) = n_0 e^{-U(x, y, z)/k_B T}, \]

assuming \( U = 0 \) and \( n = n_0 \) at the origin, where \( n_0 \) is the peak particle density. The density may be integrated over all space to find the total particle number:

\[ N = \int d^3 x n(x, y, z) = n_0 \int_{U < \frac{1}{\eta} U_{\text{max}}} d^3 x e^{-U(x, y, z)/k_B T}. \]

We then define the effective volume over this inhomogenous particle distribution to be:

\[ V_{\text{eff}} = \int_{U < \frac{1}{\eta} U_{\text{max}}} d^3 x e^{-U(x, y, z)/k_B T}. \]

iii) Gravitational Compensation

Gravity, of course, is ever-present and must be compensated somehow by the magnetic trap. Using the fact that \( F = -\nabla U \) for a conservative potential \( U \), we may balance the magnetic force against the gravitational force to find the minimum field gradient necessary:

\[ \frac{\partial B}{\partial y} = \frac{mg}{\mu}, \]

where \( m \) is the atomic mass, \( g \) is the gravitational acceleration, and the force of gravity has been chosen to lie in the \( y \) direction.

iv) Trap Frequency

For small enough displacements about a minimum, any trap may be approximated as harmonic. The trap frequency along any given direction may then be found from the field curvature in that direction:

\[ \omega_i = \sqrt{\frac{1}{m} \frac{\partial^2 U}{\partial x_i^2}} = \sqrt{\frac{\mu}{m} \frac{\partial^2 B}{\partial x_i^2}}. \]
2. The Atom Chip

The old chip has served the experiment well thus far. However, a number of design limitations exist which make the fabrication of a new chip desirable.

![Picture of new chip](image1.png)

**Figure 1:** Picture of new chip

![Diagram of new chip](image2a.png)

**Figure 2a:** Diagram of new chip (dimple wires not included)
2.1 Designing a New Chip

In designing a new chip, there are several features that we would like to improve upon from the old chip (current capacity, optical access, potential smoothness and microwave transmission), and several new features that we would like to introduce (3-wire potential, controlled dimple potential, side-wires, and the attachment of a mirror to the chip surface).

i) Current Capacity

As the magnetic field strength $B$, gradient $B'$, and curvature $B''$ are all proportional to the current $I$, increasing the current capacity of the chip wires allows for greater trap depth and confinement. Furthermore, as the current capacity is limited by the heat production of the chip wires, the chip must be able to transfer this heating to the substrate and the stack structure that supports it. The rate of temperature increase when a current $I$ is passed through a chip wire is given by [14]:

$$\frac{dT}{dt} = \frac{\rho j}{2\pi \lambda t},$$  \hspace{1cm} 14.

Where $\rho$ is the resistivity of the conductor at an initial cold temperature, $j$ is the current density, $\lambda$ is the heat conductivity of the...
substrate, and \( t \) is the time since the current has been turned on. Therefore, in order to minimize heat production, Ag (\( \rho = 1.63 \Omega m \)) is chosen as the chip wire material over Au (\( \rho = 2.2 \Omega m \)) which is used on the old chip. Also, a switch is made from a SiO\(_2\) substrate (\( \lambda = 1.3W m^{-1} K^{-1} \)) to a AlN substrate (\( \lambda = 150W m^{-1} K^{-1} \)).

**ii) Optical Access**

On the old chip, the wire pattern lies on the same side of the chip as the leads. The leads are connected to the old chip via large Macor clamps that obstruct certain optical paths. The new chip, however, employs a substrate with gold vias that provide regularly spaced conduction paths from one side of the chip to the other. This allows the leads to be connected to the back-side of the chip, keeping the front-side free of any obstruction.

![Figure 3: Back-side view of via-substrate (photo courtesy of B. Cieslak)](image)

**iii) Chip Mirror**

By removing obstructions from the front-side of the chip, new imaging and trap geometries are possible. A reflecting dielectric layer may be attached to the front-side of the chip, allowing for the option of reflective imaging as well as for the creation of standing-wave potentials.

**iv) Microwave Wires**

When the nuclear spin of an atom is coupled to the angular momentum of a valence electron (the hyperfine interaction), the ground state of each atom is split. The ground state splitting difference is 6.8
GHz for $^{87}\text{Rb}$ and 1.3 GHz for $^{40}\text{K}$. Because of the large difference in hyperfine splitting energies, each atom may be selectively targeted, for instance, allowing for selective evaporation. Or, by targeting different hyperfine levels, one may create atoms in certain spin states, opening the door for the investigation of spinor condensates.

The new chip is designed with two dedicated microwave lines. The first microwave line - designed for the 1.3 GHz transition - is simply a single wire that connects lead to ground, with a terminating resistor to be placed in between. The second microwave line - designed for the 1.3 GHz transition - is modeled after a transmission line with a lead wire between two ground wires.

v) Side-wires

Side-wires are included to simulate the Ioffe field $B_{\text{Ioffe}}$ and to provide a confining potential along the longitudinal trap axis. A constant Ioffe field keeps the trap minimum at a non-zero value, preventing spin-flip losses.

vi) 3-Wire Modulated Potential

The most significant design difference between the new and old chip is the ability of the new chip to create a modulated trapping potential. This idea, first suggested in [15] and realized in [16], makes possible the creation of elongated traps with high aspect ratios, allowing for the realization of low-dimensional condensates – an idea the group wishes to explore.

One of the present limitations of chip traps stems from the sensitivity of the atoms to chip fabrication defects. That is, because atoms lie so close to the chip surface, any wire roughness is translated into a noticeable potential roughness, affecting (especially) the smoothness of the potential along the longitudinal axis. This hinders the ability of the chip to make non-fragmented, elongated atom clouds. However, this problem may be side-stepped if a 3-wire (Z-wire + two
U-wires) potential is used instead of the Z-wire + $B_{\text{bias}}$ field potential of the old chip.

In the 3-wire configuration, current through the two U-wires create a field that is canceled by the Z-wire field some distance above the chip plane. The new chip may also be operated in the configuration of the old chip: a field from the Z-wire balanced by a bias field created from external coils.

As we are concerned with creating a smooth potential in the longitudinal direction, consider the trapping potential in this same direction:

$$U = \mu B_x^{\text{eff}} + B_{\text{bias}}^x,$$

where $B_x^{\text{eff}}$ is a constant field produced by either the Side-wires of the new chip, or the external coils of the old chip, and $\delta B_x$ is the small field produced by the roughness of the central wires in figures 4a,b. Using the 3-wire configuration, we can remove this roughness effect by alternating the current in all 3 central wires at some frequency - slow enough to for the magnetic moment to follow the field adiabatically (in order to prevent spin-flip transitions), yet fast compared to the transverse oscillation frequency (so that the atomic motion cannot follow). This results in a time-averaged potential felt by the atoms that is independent of any fabrication imperfections:
\[ U = \langle U \rangle = \mu \left( B_x^{\text{offe}} + \delta B_x \cos \omega t \right) \]

\[ = \mu B_x^{\text{offe}} \sqrt{1 + 2 \frac{\delta B_x}{B_x^{\text{offe}}} \cos \omega t + \left( \frac{\delta B_x}{B_x^{\text{offe}}} \right)^2 \cos^2 \omega t} \]

\[ = \mu B_x^{\text{offe}} \left( \frac{1}{32} \frac{\delta B_x^4}{B_x^{\text{offe}}^3} \right). \tag{15} \]

In principle, this idea is possible in the Z-wire + B\text{bias} configuration of the old chip. However, the size and strength of the bias coils needed to produce an adequate field (~20G) prohibit the high frequencies necessary (~kHz) for such a scheme to work in practice.

**vii) Dimple Wires**

Two dimple wires that lie between the Z and U-wires were added to the new chip in order to create a local dip in the \( \hat{x} \) direction potential.

![Figure 5: dimple wires between Z and U-wires](image)

The dimple wire segments in the \( \hat{x} \) direction have equal and opposite currents flowing through them, canceling the magnetic fields produced by each other in the \( z = 0 \) plane. Current flows in the same direction in the \( \hat{z} \) wire segments, however, creating a field that can either add to, or subtract from, the Side-wire field.
**Figure 6**: Field magnitude in $\hat{x}$ direction for a) 1 mA dimple current, b) no dimple current, c) –1 mA dimple current.

### 2.2 Modeling of the Atom Chip

In order to determine the geometry of the potential produced from the new chip, a Mathematica model is created. Two trapping configurations are presented: a Z-wire + $B_{\text{bias}}$ configuration for the capture of laser-cooled atoms and evaporation, and a 3-wire modulated potential for making elongated atom clouds.

A thin-wire assumption is made in order to simplify calculations. This approximation is checked by comparing the field from an infinitely-long thin-wire (eq. 7) to that of an infinitely-long, broad wire of width $w$ [14]:

$$B(z) = \mu_0 I \frac{\pi}{2w} \left( \frac{\pi}{2} - \arctan \frac{2z}{w} \right).$$

For typical values ($w = 50\mu m$ and $z = 100\mu m$) the difference of the field strength, field gradient and field curvature between the two representations is found to be 2%, 5%, and 11% respectively. This error is deemed to be acceptable for design purposes.
Figure 7: Field magnitudes along various axes for the Z-wire + $B_{\text{bias}}$ configuration (a,b,c,d) and the 3-wire configuration (e,f,g,h). Plots a) and e) show the field magnitude in the yz plane at x=0 (darker shades corresponding to weaker fields). Plots b) and f) show the field magnitude in the y direction, above the chip center (x=0, z=0). Plots c) and g) show the field magnitude in the longitudinal direction at (y=200\(\mu\)m, z=0) and (y=80\(\mu\)m, z=0) respectively. Plots d) and h) show the field magnitude in the xz plane at y=200\(\mu\)m and y=80\(\mu\)m respectively. Plots for the Z-wire + $B_{\text{bias}}$ configuration are calculated using $B_{\text{bias}} = 20G$, $B_{\text{Ioffe}} = 0G$, and $I_{Z\text{-wire}} = 2A$. Plots for the new chip are calculated using $I_{Z\text{-wire}} = 5A\cos(\omega t)$, $I_{U\text{-wire}} = 6.5\cos(\omega t)$, $I_{\text{side-wire}} = 10A$, and a modulation frequency $\omega$ much faster than the transverse trap frequency.

The first thing to notice about these plots is the difference in the position of the trap minimums: the field magnitude in the $\hat{y}$ direction of the Z-wire + $B_{\text{bias}}$ configuration has a minimum at y=200\(\mu\)m, compared with the 3-wire minimum at y=80\(\mu\)m. Also, whereas the field magnitude approaches $B_{\text{bias}}$ as $y \rightarrow \infty$ for the Z-wire + $B_{\text{bias}}$ configuration, there is a “roll-over” point at y=175\(\mu\)m for the 3-wire potential, above which, atoms are no longer trapped. This fact will limit the effective volume of the trap, and thus, the number of atoms that may be captured by it. For this reason, the chip is designed to operate in the Z-wire +
configuration just after laser cooling in order to maximize the number of
magnetically trapped atoms, and in the 3-wire configuration only after
evacative cooling.

Also, there is a noticeable trap “twist” in the Z-wire + \( B_{\text{Bias}} \)
configuration. This is caused by the presence of the \( \hat{z} \)-direction segments of the
Z-wire, which a trap minimum will stay away from. Conversely, the 3-wire
configuration has a small “twist” in the opposite direction – a consequence of
the longitudinal potential being dominated by the side-wire field.

2.3 Trap Properties

Given the different operating circumstances of the Z-wire + \( B_{\text{Bias}} \) and 3-
wire configurations, there are different trap properties that are relevant to know
for each. In the Z-wire + \( B_{\text{Bias}} \) operation mode, we would like to know the trap
depth in order to find the maximum temperature of atoms that we may trap. We
would also like to know the effective volume of this trap in order to find the
maximum number of atoms we may capture at this temperature. In the 3-wire
operation mode, we would like to know what the trap frequencies are.

\begin{enumerate}
  \item \textit{Trap depth (Z-wire + \( B_{\text{Bias}} \) configuration)}:
    \[ U_{\text{max}} / k_B = 1.3 \text{mK} \]

  \item \textit{Effective Trap Volume (Z-wire + \( B_{\text{Bias}} \) configuration)}:
    
    The effective trap is calculated analytically, approximating the potential
to be separable:
    \[ U(x, y, z) = U_x(x)U_y(y)U_z(z), \]
    then approximating \( U_x(x) \), \( U_y(y) \), and \( U_z(z) \) as triangular
potentials:
    \[ U_x(x) = ax \]
    \[ U_y(y) = by \]
    \[ U_z(z) = cz. \]
    We then find the effective volume to be:
\end{enumerate}
\[
V_{\text{eff}} = \left( \int_{U<U_{\text{max}}} \frac{dxe}{k_B T} \right) \left( \int_{U<U_{\text{max}}} \frac{dye}{k_B T} \right) \left( \int_{U<U_{\text{max}}} \frac{dze}{k_B T} \right) = 5 \cdot 10^6 \mu \text{m}^3.
\]

iii) Trap frequency (3-wire)

- strong axis: \( \nu = 21.8\text{kHz} \)
- weak axis: \( \nu = 1.1\text{kHz} \)

3. Fabricating the Atom Chip

3.1 Introduction to Optical Lithography and Metal Evaporation

Once a chip has been designed, it is fabricated in a clean-room using the techniques of optical lithography and metal evaporation. Optical lithography allows for the creation of structure sizes down to \(~1\mu\text{m}\) over a large spatial area (~cm\(^2\)). Metal evaporation allows for the deposition of different types of metals onto a lithographed pattern, up to \(~5\mu\text{m}\) in height within a few hours, with comparable resolution to the optical lithography process. The steps of lithography are shown in fig. 8.

An AlN substrate is first cleaned and prepared (a). Photoresist fluid is then applied on top of a substrate with a spinner (b), then subjected to UV light through a mask pattern of the chip design (c). The substrate is then submersed in a developer solution, which either removes the section of photoresist that has been subjected to the UV light, or removes the section that has not been subjected to the UV light (d), depending on whether a positive or negative photo-resist is being used. A negative photo-resist was used in our procedure. After a successful photo-resist pattern has been establishes on the substrate, the substrate is placed in an Electron Beam Evaporator where metal is deposited onto the substrate surface. This process is shown in fig. 9.
The evaporator deposits a metal layer onto the chip (f) by subjecting a metal sample to an electron beam. The chip is then removed from the evaporator when the desired metal thickness has been achieved and submersed in a *lift-off resist* solution. The lift-off resist attacks and dissolves the remaining
layer of photo-resist, removing the metal layer attached to it as well (g). Only a pattern of metal wires is left on the chip substrate.

### 3.2 Fabrication Apparatus

#### i) Clean-room

In order to minimize the effect of contaminants on the fabrication procedure, all work is carried out in the clean-room of the Emerging Communications Technologies Institute (ECTI) in the Bahen Centre at the University of Toronto.

A clean-room is classified according to the number of particles per square foot that are present within it. For instance, the ECTI clean-room has a class 1000 room (1000 particles/ft$^3$) in which optical lithography is carried out, and a class 10000 room (10000 particles/ft$^3$) in which evaporation is done. In addition, a majority of the lithography procedures (a, b, d, and g) take place under a fume-hood in which a High Efficiency Particulate Air (HEPA) filter creates a local class 10 clean-space.

#### ii) Spinner

The function of the spinner is to apply an even layer of photo-resist onto the substrate. This is accomplished by placing the substrate onto the middle of a rotating disk. A small amount of photo-resist is poured onto the substrate, and the spinner is rotated at some angular velocity for a certain amount of time. A thin layer of photo-resist (~1-7µm) is left on the substrate after spinning. The Spinner used was a Laurell Technologies WS-500-6NPP/LITE.

#### iii) Mask

The mask is a thin piece of glass with a chrome design pattern on one side that absorbs UV light. Our photo-mask was created by………

#### iv) Mask Aligner

A mask aligner is used to align the mask with the edges of the substrate
and control the exposure of the photo-resist to UV light. The mask aligner used was a KarlSuss MA 6 with an i-line ($\lambda=365\text{nm}$) intensity of $20\text{W/cm}^2$ and an h-line ($\lambda=405\text{nm}$) intensity of $15\text{W/cm}^2$. Vacuum side channels hold the mask in place while it is being aligned with the chip with the aid of a microscope objective. A Wedge Error Correction (WEC) is then performed by the aligner to make sure that the chip plane is parallel to the mask plane.

The exposure mode, as well as its duration, is then chosen from the following options:

1) Proximity Exposure
   In this exposure mode, the mask is held a given distance away from the substrate. There is no risk of damage to the mask, however the pattern resolution is somewhat compromised.

2) Soft Contact Exposure
   In this exposure mode, the mask is brought into light contact with the substrate. Some risk of damage to the mask exists and pattern resolution is better than with proximity exposure (typically 1-2$\mu$m).

3) Hard Contact Exposure
   In this exposure mode, the substrate is pressed into contact with the substrate. This mode allows for the best resolution, yet places the mask in the most danger of being damaged.

*Electron Beam Evaporator*

Metal is evaporated onto the chip using a BOC Edwards E-beam evaporator. A chip sample is placed into the evaporator chamber and the chamber is pumped down below $10^{-5}$ Torr. An electron beam is produced from a filament and directed onto the metal sample, heating it past its boiling point. The amount of metal that has been evaporated is checked using a calibrated thickness monitor positioned inside the evaporation chamber.
3.3 Fabrication Materials

Photo-resist, Developer and Lift-off Resist:

The photo-resist chosen for our fabrication procedure was AZ nLOF 2070, a negative photo-resist that chemically responds to i-line radiation. This is the most viscous of the AZ nLOF 2000 series resists, a product that has been used successfully in the AtomChip group in Vienna and the Orsay atom chip group in France, and therefore allows the largest spin-on thickness – up to 7µm. Also, being a negative photo-resist, any light divergence during exposure will produce an undercut profile – a profile in which the bottom of the photo-resist is less wide than the top of the photo-resist. This profile makes it easier for the lift-off resist to attack and remove the photo-resist after metal evaporation. Product details for this resist may be found in Appendix A.

The developer used was AZ 300 MIF, recommended as a compliment to the AZ nLOF 2070 resist. The lift-off resist used was acetone.

Metals

When considering which metals to use, a number of factors were considered: electrical resistivity, thermal conductivity, oxidation energy, vapor pressure, melting point, and cost. A list of these quantities for Ag, Au, Cu, and Al is given in [20]. The resulting choice was for Ag, which had the best combination of properties. As well, Cr and Ti were chosen as adhesion/base layers, and a thin gold coating was evaporated on top of the silver layer in order to prevent oxidation.

3.4 Fabrication Procedure

General Considerations

The primary concern when fabricating small-scale structures such as atom chips is cleanliness. As such, separate and dedicated Petri dishes are used for each step: eg. There is one dish for acetone, one for the AZ 300 MIF developer, one for isopropanol, etc.. Dishes and tweezers are cleaned after each use. The mask is inspected before each exposure, and cleaned
with acetone, methanol and a q-tip when necessary.

Substrate Preparation

Before optical lithography is undertaken, the substrate is first cleaned with a Piranha etch solution (3 parts sulfuric acid + 1 part hydrogen peroxide), and then with acetone and methanol in a sonic bath should a significant time elapse until lithography.

In beginning fabrication attempts, the substrates were cleaned with only acetone and methanol. Good lithography patterns were achieved, however, metal was unable to adhere well to the substrate during the evaporation stage. Cleaning in a Piranha etch solution solved this problem, but had the tendency to remove grains from the surface of the substrate, creating surface roughness. This second problem was minimized if a substrate was subjected to the Piranha etch solution for less than 120s.

After Piranha etch and acetone+methanol cleaning, the substrate is rinsed in de-ionized water, blown dry with nitrogen gas, then baked on a hotplate at 100°C for a ~3 minutes to remove any remaining moisture.

Figure 10: Close-up photos of the chip centre: a) Piranha-cleaned chip after
lithography, b) Piranha-cleaned chip after metal evaporation, c) Non-Piranha-cleaned chip after lithography, d) Non-Piranha-cleaned chip after metal evaporation.

*Lithography Procedure*

After the substrate has been cleaned, it is ready for lithography. The successful procedure used is given below:

1) **Spin on resist** – pour photo-resist onto the substrate, spin at 1000rpm for 10s, then 4000rpm for 30s. The first spin rate is thought to spread the resist evenly, while the second spin rate removes resist to a thickness of 6µm.

2) **Remove excess resist from substrate edges** – this is done with acetone and a q-tip. During spinning, resist collects near the edges of the substrate. In order to make sure that the mask aligner brings the mask into close enough contact with the mask during exposure, this bead of resist is removed.

3) **Softbake** – the substrate is then baked on a hotplate for 6 minutes at 100°C. This time is based on the rule [17]: 1 minute of softbake at 100°C per µm of photoresist. The substrate is allowed to cool.

4) **Exposure** – the mask and substrate are loaded into the mask aligner where the substrate is exposed to 11s of UV light in Hard-contact mode.

5) **Post-Exposure Bake** – the exposed substrate is baked on a hotplate at 100°C for an additional 60s. The substrate is allowed to cool.

6) **Development** – the substrate is placed in a Petri dish of AZ 300 MIF developer for ~120s, or until all chip features have been resolved.

7) **Rinse and Dry** – as soon as features have been resolved, the substrate is immediately placed in de-ionized water to stop development. The substrate is then rinsed with de-ionized water and blown dry with nitrogen.
At this point, the substrate is checked with a microscope to see if a satisfactory pattern has been achieved. If so, the substrate is ready for the metal evaporation stage.

**Metal Evaporation Procedure**

One critical parameter noticed to have a dramatic affect on the evaporation quality was the wait time between lithography and evaporation. Any evaporation trials taking place within 12 hours of lithography seemed to melt the photo-resist. Likewise, any evaporation trials completed after 2 days had elapsed since lithography turned out poorly because of problems with the lift-off resist dissolving the photo-resist. Therefore, all evaporation trials were conducted 24 hours after a successful lithography run. The procedure for evaporation is as follows:

1) **Loading the substrate and metals** – the substrate is pinned, upside-down, to a holding stage at the top of the evaporation chamber. Cr, Ti, Ag, and Au are loaded in their respective crucibles into the chamber.

2) **Calibrating the thickness monitor** – measurements of the crucible, substrate, and thickness monitor positions are taken. This data is used to find a tooling factor that translates the thickness measured on the monitor to the thickness deposited onto the chip.

3) **Pump-down** – the evaporator chamber is sealed and pumped down below $10^{-5}$ Torr. This takes between 1 and 2 hours.

4) **Metal evaporation** – the electron beam is powered on and metal is evaporated onto the chip at the following rates, times, electron beam currents, and thickness:

<table>
<thead>
<tr>
<th>Metal</th>
<th>E-beam current (mA)</th>
<th>Rate (nm/s)</th>
<th>Time (min)</th>
<th>Thickness (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cr</td>
<td>5 (soak) 30 (evap)</td>
<td>.80</td>
<td>5</td>
<td>400</td>
</tr>
</tbody>
</table>
Lift-Off Procedure

After metal evaporation, the chip is ready for lift-off. Lift-off quality does not seem overly sensitive to the elapsed time since evaporation. The procedure is as follows:

1) **Lift-off resist** – the substrate is placed in a warm acetone bath in a sonic agitator for 15-30 minutes.
2) **Lift-off rinse** – after metal has been removed by the acetone, the substrate is rinsed with isopropanol.
3) **Rinse and dry** – the substrate is then rinsed in de-ionized water and blown dry with nitrogen. Steps 1-3 are repeated, as necessary.

<table>
<thead>
<tr>
<th></th>
<th>0 (cool-down)</th>
<th>5</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Ti</strong></td>
<td>5 (soak)</td>
<td>5</td>
</tr>
<tr>
<td>120 (evap)</td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>0 (cool-down)</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>130 (evap)</td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>0 (cool-down)</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td><strong>Ag</strong></td>
<td>5 (soak)</td>
<td>5</td>
</tr>
<tr>
<td>100 (evap)</td>
<td>1.60</td>
<td></td>
</tr>
<tr>
<td>0 (cool-down)</td>
<td>35</td>
<td></td>
</tr>
<tr>
<td><strong>Au</strong></td>
<td>5 (soak)</td>
<td>5</td>
</tr>
<tr>
<td>230 (evap)</td>
<td>0.01</td>
<td></td>
</tr>
<tr>
<td>0 (cool-down)</td>
<td>30</td>
<td></td>
</tr>
</tbody>
</table>

**Total:**

4.4 µm

5) **Cool-down** – the electron beam is powered off and the chamber is allowed to cool off before the chip is removed.
Checking the Wire Height

The thickness monitor on the evaporator gives a rough approximation of the wire height, but the height can be checked more accurately with the use of a profilometer:

![Figure 11: Profilometer measurement of chip wire height. Profilometer begins on a wire, encounters a \(~4\mu m\) step down to the substrate, then climbs back up to another wire.](image)

Problems and Solutions

The lithography process is very sensitive to such variables as how centered the substrate is on the spinner, how quickly one moves from one step to the next, how well one is able to control the temperature of the substrate, how evenly resist is removed from the edge of the substrate, etc. Results became more and more reliable the better one became at these particulars. One problem of note is the unwanted deposition of metal to the sides of the substrate that always occurs during evaporation. This causes a shorting among the wires. The easiest solution is to proceed with evaporation as normal, then test all connections for shorts after lift-off, manually removing any offending sections of metal with a sharp razor blade when necessary.

3.5 Mirrorizing the Chip

After a metal wire pattern has been produced on the substrate, a reflecting dielectric is attached to the top of it. This is done with a 353ND epoxy from Epoxy Technologies. The dielectric is attached to the top of the
chip with a model 353ND epoxy from Epoxy Technology. The epoxy is designed to fill in channels caused by the wire pattern on the chip. Multiple epoxy/dielectric layers may be necessary to reach the desired flatness. The procedure for attaching the dielectric to the chip is given below.

1) **Apply epoxy to the chip** – a couple drops of epoxy from the tip of a syringe or small wire (~100µm diameter) are applied to the middle of the substrate.
2) **Dielectric is lowered onto chip** – using an aluminum press (made by Dave McKay), the dielectric is lowered onto the substrate. A weight on top of the press applies pressure.
3) **Cure epoxy** – the press/substrate/dielectric combination, already positioned on a hot plate, is heated to ~150°C for 40 minutes. The substrate is then allowed to cool overnight.
4) **Separate dielectric from glass substrate** – the substrate is manually removed from the glass with the dielectric attached.

*Problems and Solutions*

The dielectric-to-glass adhesion strength is comparable to the metal-to-substrate adhesion strength. Therefore, it is often the case during step 4) that the metal is separated from the substrate rather than the dielectric being separated from the glass. This problem is mitigated when a long cooling period after step 3) is allowed, and an even separating force is applied over the whole chip in step 4).

### 4. Coupling to the Experiment

After a chip has been fabricated, it is ready to be incorporated into the experiment. This involves securing the chip to a new stack, connecting wire leads to the chip vias, determining the microwave transmittance, and vacuum
testing all components in a test vacuum chamber beside the working experiment.

4.1 Connecting the Chip to the Stack

The stack to which the new chip is to be connected was designed and constructed by Dave McKay in 2006 [18]. The stack itself is a single Cu structure consisting of a platform on which the chip is to be secured, wire feedthroughs that allow the transmittance of electrical signals from outside the vacuum to the chip, and a vacuum flange on which the whole stack is mounted.

Building a new stack was necessary in order to accommodate the extra wire connections present on the new chip (24 connections vs. 8 on the current chip) as well as the high frequency (GHz) signals that the new chip is designed to use. Consequently, the chip was designed with anodized aluminum wire channels to house Cu wires (for the DC and low frequency chip wires) and double-shielded RG-142 co-axial cable (for high frequency chip wires).

The chip is connected to the stack with a thermally conductive H77 epoxy from Epoxy Technologies.

4.2 Connecting Leads to the Chip: DC and Low Frequency Signals

First attempts at connecting lead wires to the chip-via contact pads used a low out-gassing, vacuum compatible solder. However, due to the high thermal conductivity of the AlN substrate, forming reliable wire connections was found to be difficult. Therefore, a thermally and electrically conductive vacuum compatible H21D epoxy from Epoxy Technologies was chosen. A resistance of 0.1Ω was measured when a 10A DC current was passed through a cured epoxy contact that had been appropriately heat-sunk. This was comparable to the measured resistance of the vacuum solder.
4.3 Connecting Leads to the Chip: Microwave Frequency

When frequencies become large enough that their wavelengths are comparable to the system size, care must be taken to ensure that the epoxy contacts and microwave chip wires still transmit signals well. This means having enough current amplitude $I$ through the microwave chip wire to generate a sufficiently high Rabi frequency $\Omega_R$:

$$\hbar \Omega_R = \mu_B B$$  \hspace{1cm} 20.

where $\mu_B$ is the Bohr magneton and $B = \frac{\mu_0 I}{2\pi r}$. The current, however, may be attenuated, or reflected, by any of the circuit elements in its path – this includes the epoxy contacts, any resistors or capacitors used to terminate the transmission line, and the chip wires themselves. Therefore, it is necessary to test the epoxy contact and microwave chip lines to see what sort of high frequency behaviour they each have. This was done in two different ways:

i) Measuring the reflected power

When an oscillating signal propagates through a transmission line of impedance $Z_0$, it will eventually reach the end and see either a short, open circuit, or some kind of terminating load impedance $Z_L$. Some fraction of the wave will be reflected at this point, according to the reflection co-efficient $\Gamma$:

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0}$$  \hspace{1cm} 21.

Therefore, if we want to maximize to the fraction of the wave that is transmitted, we want to minimize $\Gamma$ by choosing a load impedance equal to the transmission line impedance. Recall that this load impedance includes the epoxy contact, chip wire, plus any circuit element we choose to add. For simplicity, the chosen circuit element as we choose is a resistor.

In order to measure the reflected power, a Minicircuits ZEDC-110 directional coupler is used. The directional coupler is a 3-port device able to distinguish between a forward propagating, and backward, propagating wave - directing the reflected wave to a spectrum analyzer. The spectrum analyzer
measures the power of the reflected wave for different load resistors over a 600-1000 MHz frequency range. A schematic of this set-up may be seen in figure 11. Measured results may be seen in figure 12.

![Circuit set-up for measuring the reflected power from the chip.](image)

**Figure 11:** Circuit set-up for measuring the reflected power from the chip. The signal enters through the “out” port of the Directional Coupler, travels out through the “in” port with minimal loss (1dB), encounters the chip and part of the signal is reflected back upon itself through the “in” port and out the “cpl” port to the Signal Analyzer.

![Graph of reflected power vs. frequency for various resistive loads.](image)

**Figure 12:** Reflected power vs. frequency for various resistive loads. The dips in power were first thought to be standing wave phenomenon. However, subsequent measurements, in which the cable length was varied, was not able to verify this.

**ii) Measuring the Chip Impedance**

While measuring the reflected power gives some insight into the resistive behaviour of the chip + epoxy contacts, nothing has been learned of the
chip’s reactive nature. A full analysis of the complex impedance requires a microwave network analyzer.

5. Conclusion and Future Work

Since the beginning of January, when work towards the fabrication of an atom chip started in earnest, much has been accomplished: multiple atom chips have been successfully patterned, reliable lead connections have been made, and a model of the chip has been computed.

Specific problems remaining include the characterization of the chip impedance at 1.3 GHz and 6.8 GHz, and developing a more reliable mirrorizing procedure. The former problem requires a Network Analyzer and someone to staff it, the latter problem requires more tweaking of the procedure. Finally, when the time is right, the current experiment will be opened up and the new chip and stack will be integrated into it.

Bibliography


[13] L. Leblanc, Evaporative Cooling in a Strongly Confining Microchip Trap, University of Toronto, 2005


[18] D. McKay, Microwave manipulation of atoms on a chip, University of Toronto, 2005
Appendix: AZ nLOF 2000 Series Data Sheets

AZ nLOF 2000 Series
Summary

Process capability:
0.7µm CD @ 2.0 µm FT
0.9µm CD @ 3.5 µm FT

AZ nLOF 2020: For 2.0 µm FT, DTP = 66 mJ/cm²
AZ nLOF 2035: For 3.5 µm FT, DTP = 80 mJ/cm²
AZ nLOF 2070: For 7.0 µm FT, DTP = 180 mJ/cm²
AZ nLOF 2070
Baseline Process for 7.0 μm FT

Coated Thickness: 7.0 μm
Softbake: 110°C/90 sec - Contact mode
PEB: 110°C/90 sec - Contact mode
Exposure: ASML i-line, 0.60 NA
Develop: 120 sec double-pan in
AZ 300 MIF Developer @ 23°C
Data: On following page